Central™
Semiconductor Corp.

PROCESS CP208

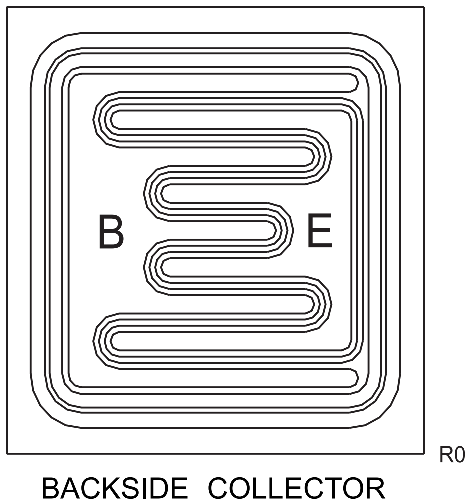
Power Transistor

NPN - Amp/Switch Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL BASE
Die Size	66 X 66 MILS
Die Thickness	12.5 ± 1.0 MILS
Base Bonding Pad Area	12 X 24 MILS
Emitter Bonding Pad Area	11 X 14 MILS
Top Side Metalization	Al - 50,000Å
Back Side Metalization	Cr/Ni/Ag - 16,000Å

GEOMETRY



BACKSIDE COLLECTOR

GROSS DIE PER 4 INCH WAFER

2,630

PRINCIPAL DEVICE TYPES

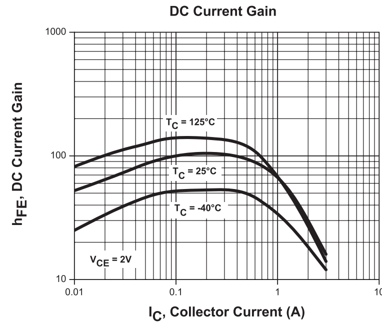
CJD31C
MJE182
TIP31C

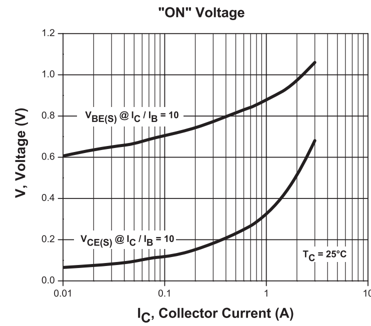
145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

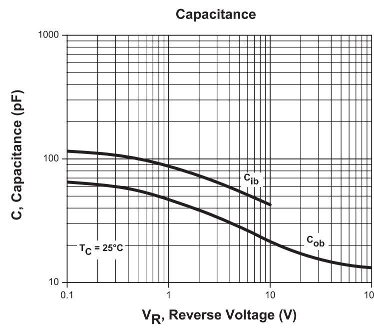
R3 (16-August 2006)

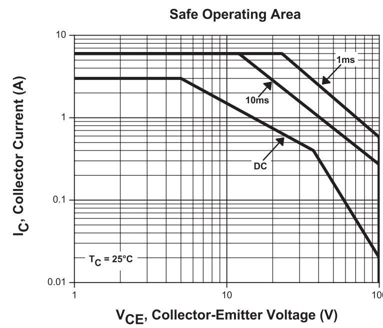
PROCESS CP208

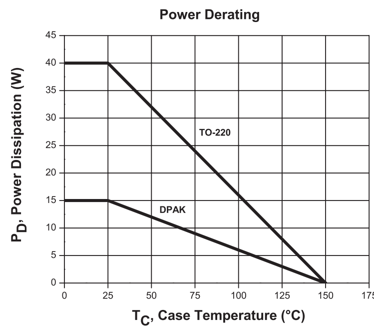
Typical Electrical Characteristics

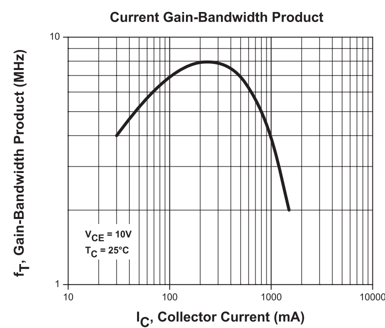












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